

Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Currently Amended)* A circuit arrangement having at least one phase locked loop comprising:

at least one phase detector for detecting phase information of at least one analog input signal ~~in particular following the arrival of at least one rising edge and/or falling edge of at least one analog input signal;~~

at least one loop filter to which the output signal which is output by the phase detector ~~can be~~ is fed, for determining at least one increment~~[[,]]~~; ~~and~~

at least one ramp oscillator to which the increment which is output by the loop filter ~~can be~~ is fed, characterized in that the phase locked loop ~~is essentially digital and for this reason may have comprises~~ at least one time-to-digital converter to which at least one system clock ~~can be~~ is fed, for digitizing the input signal in particular the phase of the input signal;

wherein the phase detector ~~can be~~ is fed the output signal ~~in particular the~~ , including additional phase information, of the time-to-digital converter and also at least a first output signal in particular at least one status signal, of the ramp oscillator; and

at least one frequency detector ~~can be~~ is fed at least a second output signal in particular at least one overflow pulse~~[[,]]~~ of the ramp oscillator and outputs frequency information to the loop filter which ~~may also be~~ is assigned to at least one frequency locked loop.

2. *(Currently Amended)* A circuit arrangement as claimed in claim 1 wherein , ~~characterized in that~~ at least one splitter unit in particular signal splitter, which ~~can be~~ is fed:

[[~~-~~]]the increment of the loop filter;

[[~~-~~]]the first output signal of the ramp oscillator; and

[[~~-~~]]the second output signal of the ramp oscillator determines there from at least one digital output signal in particular the digital phase of at least one digital output signal; ~~and~~

wherein at least one digital-to-time converter which ~~can be~~ is fed the second output signal of the ramp oscillator converts the digital output signal into at least one analog, in particular time-dependent, output signal.

3. (Currently Amended) A circuit arrangement as claimed in claim 1, characterized in that at least one analog phase locked loop in particular for multiplying the output frequency, is connected downstream of the digital-to-time converter~~[[,]]~~; and

the output signal of the analog phase locked loop passes to at least one frequency generator in particular to at least one frequency splitter, in order to generate at least one output signal of the circuit arrangement.

4. (Currently Amended) A circuit arrangement as claimed in claim 3, characterized in that the phase locked loop has at least a second phase detector which ~~can be~~ is fed ~~[[,]]~~ the first output signal of the ramp oscillator and ~~[[,]]~~ at least one output signal of the output signals sent out by the frequency generator; and

wherein at least a fourth adder connected between the first phase detector and the loop filter for adding the output signal of the first phase detector to the in particular negative output signal of the second phase detector.

5. (Currently Amended) A circuit arrangement as claimed in claim 4, characterized in that the phase locked loop has at least a second time-to-digital converter which ~~can be~~ is fed the output signal of the frequency generator and the output signal of which ~~can be~~ is fed to the second phase detector.

6. (Currently Amended) A circuit arrangement as claimed in claim 3, characterized by at least a first switching element connected upstream of the time-to-digital converter and the phase detector the output signal of which first switching element ~~can be~~ is switched as a function of at least one switching signal between the input signal and at least one output signal of the output signals sent out by the frequency generator;

at least a second switching element connected between the phase detector and at least a first register element assigned to the input signal and at least a second register element assigned to the output signal of the frequency generator; and

at least a fourth adder connected upstream of the loop filter for adding the output signal of the first register element to the in particular negative output signal of the second register element;

wherein as a function of the switching signal the input of the first register element or the input of the second register element ~~can be~~ is fed the output signal of the phase detector by the second switching element;

as a function of the negated switching signal the first input of the fourth adder ~~can be~~ is fed the first output signal of the second switching element by the first register element; and

as a function of the switching signal the second input of the fourth adder ~~can be~~ is fed the second output signal of the second switching element by the second register element.

7. *(Currently Amended)* A circuit arrangement as claimed in claim 1, characterized in that the frequency locked loop has at least one increment module in particular at least one increment generation unit, and

at least one adaptation unit is connected between the increment module and the loop filter which adaptation unit ~~can be~~ is fed the increment which is output by the loop filter is designed to provide at least one adaptive algorithm and outputs at least one output signal.

8. *(Currently Amended)* A circuit arrangement as claimed in claim 1. characterized in that the loop filter ~~has~~ comprises:

at least a first proportional element for multiplying the output signal of the phase detector by at least one proportional coefficient or proportional factor[[,]];

at least one proportional path;

at least one integral path and;

at least a first adder for adding the output signal of the proportional path to the output signal of the integral path;

wherein the integral path has;

[[-]]at least a second proportional element for multiplying the output signal of the first proportional element by the proportional coefficient or proportional factor

[[-]]at least one integral element for multiplying the output signal of the second proportional element by an integral coefficient or integral factor; and

[[-]]at least one integrator intended to integrate the output signal of the integral element_said integrator[[-]] having;

at least a third adder for adding the output signal of

the integral element to the output signal of the frequency detector and to the fed-back output signal of the integrator;
[~~--~~] ~~having~~ at least one integral value limiter for limiting the output signal of the third adder; and
[~~--~~] ~~having~~ at least one delay element.

9. *(Currently Amended)* A circuit arrangement as claimed in claim 1, characterized in that the output signal of the first adder is formed as a function of the respective operating mode of the phase locked loop ~~either as claimed in claim 8~~ [~~or~~] by feeding to the integral path the output signal of the adaptation unit while at the same time feeding to the proportional path at least one vanishing signal;

at least one frequency limiter for limiting the frequency of the output signal of the first adder is connected downstream of the first adder[~~,~~]; and

at least a second adder for adding the output signal of the frequency limiter to at least one nominal increment signal is connected downstream of the frequency limiter.

10. *(Currently Amended)* A method of locking onto and/or processing ~~data, in particular audio, T[ele]V[ision]~~ television and/or video data, by means of at least one phase locked loop ~~wherein~~ the method comprising:

detecting phase information ~~is detected~~ by means of at least one phase detector ~~in particular~~ following the arrival of at least one rising edge and/or falling edge of at least one analog input signal;

determining at least one ~~increment is determined by means of~~ using at least one loop filter to which the output signal which is output by the phase detector is fed[~~,~~]; and

communicating an increment to at least one ramp oscillator is fed the increment which is output by the loop filter; ~~characterized in that~~

wherein the phase locked loop is essentially digital, wherein the input signal in particular the phase of the input signal ~~can be~~ is digitized by means of at least one time-to-digital converter to which at least one system clock is fed[~~,~~];

the phase detector is fed the output signal in particular the additional phase information, of the time-to-digital converter and also at least a first output signal in particular at least one status signal, of the ramp oscillator; and

at least one frequency detector is fed at least a second output signal in particular at least one overflow pulse, of the ramp oscillator and outputs frequency information to the loop fitter which in particular is also assigned to at least one frequency locked loop.

11. *(Currently Amended)* [[A]] The method as claimed in claim 10, ~~characterized in that further comprising:~~

communicating to at least one splitter unit ~~in particular comprising a signal splitter~~[[,]] ~~which is fed the~~ [[-]] increment of the loop filter; [[-]] the first output signal of the ramp oscillator; and [[-]] the second output signal of the ramp oscillator;

determining ~~determines there from~~ the increment, the first output signal of the ramp oscillator, and the second output signal of the ramp oscillator at least one digital output signal in particular the digital phase of at least one digital output signal;

communicating to at least one digital-to-time converter ~~which is fed the second output signal of the ramp oscillator;~~

converting ~~converts~~ the digital output signal into at least one analog, ~~in particular time-dependent~~[[,]] output signal;

multiplying the output frequency ~~is multiplied by means using~~ of at least one analog phase locked loop which is connected downstream of the digital-to-time converter; and

communicating the output signal of the analog phase locked loop ~~passes to~~ at least one frequency generator comprising in particular to at least one frequency splitter, in order to generate at least one output signal of the circuit arrangement.

12. *(Currently Amended)* [[A]] The method as claimed in claim 11, characterized in that phase information of at least one output signal of the output signals sent out by the frequency generator is determined and output by at least a second phase detector as an in particular negative output signal; and

the output signal of the first phase detector is added to the in particular negative output signal of the second phase detector by at least a fourth adder.

13. *(Currently Amended)* [[A]] The method as claimed in claim 12, characterized in that, in the event of insufficient accuracy of a system clock period as maximum phase offset between the input signal and the output signal of the frequency generator there is assigned to

the phase locked loop at least a second time-to-digital converter which is fed the output signal of the frequency generator and the output signal of which is fed to the second phase detector.

14. (Currently Amended) ~~[[A]]~~ The method as claimed in claim 11 further comprising:
~~, characterized in that as a function of at least one switching signal the output signal of at least a first~~

switching an output signal of at least a first switching element is switched between the input signal and at least one output signal of the output signals sent out by the frequency generator as a function of at least one switching signal;

communicating to the phase detector is fed the output signal of the first switching element;

assigning as a function of the switching signal at least a first register element assigned to the input signal to at least a first register element; the input signal or

assigning the output signal of the frequency generator to at least a second register element;

communicating assigned to the output signal of the frequency generator is fed the output signal of the phase detector to either the first register element or the second register element by at least a second switching element;

communicating to as a function of the negated switching signal at least a fourth adder, as a function of the negated switching signal, is fed the first output signal of the second switching element;

communicating to as a function of the switching signal the fourth adder, as a function of the switching signal, is fed the second output signal of the second switching element; and

adding the output signal of the first register element is added to the in-particular negative output signal of the second register element.

15. (Currently Amended) ~~[[A]]~~ The method as claimed in claim 10, characterized in that, in the frequency locked loop at least one adaptation unit provides at least one adaptive algorithm and outputs at least one output signal said adaptation unit being fed the increment which is output by the loop filter and being connected between at least one increment module in particular at least one increment generation unit, and the loop filter.

16. Cancelled